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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,692	03/24/2004	Yoshifumi Tanada	0553-401	4403

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,692	TANADA, YOSHIFUMI	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-19* is/are allowed.

6)☒ Claim(s) *1,5 and 20-22* is/are rejected.

7)☒ Claim(s) *2-4,6-8 and 23-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/17/06*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5 and 20-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Osada (US 2004/0119824).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In claim 1, Osada teaches all claimed features in Fig. 4A, an inspecting circuit of a semiconductor device comprising: at least first and second signal lines (S1, S2); at least first, second and third NANDs (3 NANDs, as seen from left side of Fig. 4A), each of the first, second, and third NANDs having first and second input terminals (two input terminals); and an output terminal (O) electrically connected to outputs of the first, second, and third NANDs; wherein an output of the first NAND (output from the very first

NAND from the left side) is electrically connected to the first terminal of the second NAND (as seen), wherein an output of the second NAND (output from the second NAND from the left side) is electrically connected to the first input terminal of the third NAND (as plainly seen), wherein the second input terminals of the first, second, and third NANDs are connected to first, second, and third lines (S1, S2, S3), respectively, and wherein a determination (a decision made by circuit of Fig. 4A) of whether the semiconductor device is normally operated or not is based on at least a signal obtained at the output terminal (OUT).

In claim 5, Osada teaches all claimed features in Fig. 4A, an inspecting circuit of a semiconductor device comprising: at least first, second, and third signal lines (S1, S2, S3); at least first, second and third NANDs (3 NANDs, as seen from left side of Fig. 4A), each of the first, second, and third NANDs having first and second input terminals (two input terminals); and an output terminal (O) electrically connected to outputs of the first, second, and third NANDs; wherein an output of the first NAND (output from the very first NAND from the left side) is electrically connected to the first terminal of the second NAND (as seen), wherein an output of the second NAND (output from the second NAND from the left side) is electrically connected to the first input terminal of the third NAND (as plainly seen), wherein the second input terminals of the first, second, and third NANDs are connected to first, second, and third lines (S1, S2, S3), respectively, and wherein a determination (a decision made by circuit of Fig. 4A) of whether the semiconductor device is normally operated or not is based on at least a signal obtained at the output terminal (OUT) and a reference patter (VDD).

Claim 20 corresponds to detailed circuitry already discussed similarly with regard to claim 1.

Claim 21 corresponds to detailed circuitry already discussed similarly with regard to claim 5.

In claim 22, Osada teaches all claimed features in Figs. 3A and 4A, a semiconductor device comprising: a shift register (Shift Register); and an inspecting circuit of a semiconductor device comprising: at least first and second signal lines (S1, S2); at least first and second NANDs (2 NANDs, as seen from left side of Fig. 4A), each of the first and second NANDs having first and second input terminals (two input terminals); and an output terminal (O) electrically connected to outputs of the first and second NANDs; wherein the second input terminals of the first and second NANDs are connected to first and second lines (S1, S2), respectively, wherein the first and second lines (S1, S2) are electrically connected to the shift register (via first and second latches), and wherein a determination (a decision made by circuit of Fig. 4A) of whether the semiconductor device is normally operated or not is based on at least a signal obtained at the output terminal (OUT).

3. Claims 2-4, 6-8 and 23-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 9-19 appear to comprise allowable subject matter of a source driver, which inputs a clock signal and a start pulse.

Response to Arguments

In light of further consideration, a new ground of rejection has been set forth because Osada anticipates all claimed features of claims 1, 5 and 20-22 under 35 U.S.C. 102(e), as discussed above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER